

## **REMARKS**

Claims 1-51 are pending in this Application. The Examiner issued a restriction requirement under 35 U.S.C. § 121, and Applicants elected claims 1-17. Those claims stand rejected, while claims 18-51 are withdrawn from consideration. In response to the above-identified Office Action, Applicants do not amend any claims, cancel claims, or add any new claims. Reconsideration of the rejected claims in light of the following remarks is requested.

### **I. Election/Restriction under 35 U.S.C. §121**

Applicants respectfully request election of Group I, Claims 1-17, drawn to memory access blocking and access limiting, classified in class 711, subclasses 152 and 163, for prosecution, with traverse. Claims 18-34 (Group II) and claims 35-51 (Group III) are withdrawn from consideration.

### **II. Claims Rejected Under 35 U.S.C. § 102(b)**

The Examiner rejected claims 1-17 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,343,339 issued to Daynes ("*Daynes*"). However, as explained below, *Daynes* fails to disclose some elements recited in the claims, and consequently other elements are not arranged as specified, so *Daynes* fails to anticipate the present invention.

Claim 1 recites a processor for offloading processing in a storage environment, the processor comprising several elements. First among these elements is a processor interface that interfaces the processor to a network processor configured to perform a storage function. The Examiner has identified the claimed processor as the "Processor" shown at 113 in *Daynes*' Figure 1, and the processor interface as "Comm Int" (communication interface) 120 (also *Daynes*' Figure 1). The network processor to which the processor is interfaced is said to be disclosed as one of three things in the reference: local network 122,

ISP (Internet Service Provider) 124 or Internet 125 (all references to *Daynes* Figure 1).

According to the claim, the network processor must be configured to perform a storage function, but a local network or the Internet are generally configured to transfer or communicate data, not to store it; and *Daynes* does not describe any unusual storage-type configuration of these items. An ISP sometimes provides data storage, but again, *Daynes* does not teach, suggest, mention or rely on such a configuration. Instead, the ISP “provides data communication services through the world wide packet communication network now commonly referred to as the ‘Internet.’” (*See Daynes* c. 6, ll. 35-42.) Consequently, none of *Daynes*’ local network, ISP or Internet properly anticipates the network processor recited in claim 1 because none is configured to perform a storage function.

The second element required by claim 1 is semaphore circuitry, coupled to the processor interface, that receives a signal from the network processor and controls a semaphore related to the signal for locking and unlocking access to data. The Examiner asserts that the semaphore circuitry is met by *Daynes*’ lock data structure and lock manager, and that receiving a signal from the network processor and controlling a semaphore related to the signal is described in *Daynes*’ “Lock Acquisition” section at c. 11, ll. 13-33. However, even assuming (solely for the sake of argument) that the lock data structure and lock manager properly anticipate the claimed semaphore circuitry, *Daynes* does not describe any connection, relationship or interaction between the lock structure and the local network, Internet or ISP that fulfills the “receives a signal” part of the claim.

In other words, *Daynes* does not teach or suggest that the lock data structure and lock manager receive a signal from the local network, Internet or ISP, and therefore does not teach/suggest controlling a semaphore *related to said signal* for locking and unlocking access to data, so *Daynes*’ structures that allegedly anticipate the claim elements are not arranged as they are in the claim.

For at least these reasons, Applicants respectfully submit that the reference of record fails to anticipate the claimed invention, and request that the rejection be withdrawn.

Claims 2-10 depend directly or indirectly on claim 1, and are believed to be patentable for at least the reasons discussed above. Applicants respectfully request that the Examiner withdraw the rejections of these claims as well.

Claim 11 recites a method of controlling a processor for offloading processing in a storage environment, comprising several specified operations. The Examiner rejects this claim (and its dependent claims) “for the same reasons as stated above with respect to claims 1-10.” However, as Applicants have shown, the rejection is improper. Thus, for similar reasons, Applicants submit that claims 11-17 are patentable over the reference of record, and respectfully request that the Examiner withdraw these rejections.

The Examiner also rejected claims 1-5, 8, 11-14 and 16 under 35 U.S.C. § 102(b) as anticipated by Applicants’ Admitted Prior Art (“AAPA”). These rejections seem to be founded upon Applicants’ simple block diagram of a storage area network system, Fig. 1, in conjunction with an element allegedly labeled “semaphore circuitry.” However, no such element appears in Figure 1 (or any of the other figures), nor is any semaphore circuitry described in the Background section. Semaphore *management* is mentioned in the Background as a function that it is advantageous for a storage server to perform quickly. However, the method of performing this function is not described, except to say that it is typically performed in software. Semaphore *circuitry*, on the other hand, is described (*e.g.* in the Brief Summary) as part of the co-processor (*see* ¶ [0016]), which is itself part of a storage server according to an embodiment (*see* Fig. 2 and ¶¶ [0056]-[0064]).

Certainly, the claimed elements and interactions are described in the Detailed Description of the Invention, but the descriptions concern the storage server’s construction and internal operations. The mere fact that a prior-art

storage server is shown in a figure labeled “Prior Art” does not admit that the known storage server contains the inventive structures or that they operate as claimed.

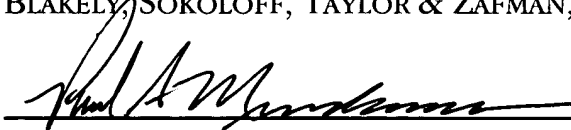
Applicants respectfully request that the Examiner withdraw these rejections of the claims over *AAPA*, or provide additional citations to elements of Figure 1 and the text describing it that allegedly establish that the described structures necessarily interact as recited in the claims.

### CONCLUSION

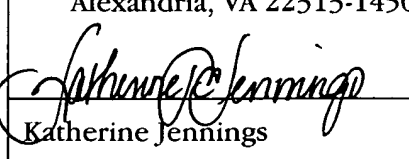
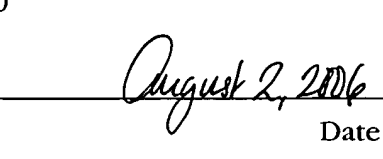
In view of the foregoing, it is believed that all claims now pending, namely claims 1-17, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Respectfully submitted,  
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<p>12400 Wilshire Boulevard Seventh Floor Los Angeles, California 90025  (310) 207-3800</p>	<p style="text-align: center;"><u><b>CERTIFICATE OF MAILING</b></u></p> <p>I hereby certify that the correspondence is being deposited with the United States Postal Service with sufficient postage for first class mail, in an envelope addressed to:</p> <p style="text-align: center;">Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450</p> <div style="display: flex; justify-content: space-between;"><div data-bbox="649 1428 1055 1585"> Katherine Jennings</div><div data-bbox="1055 1428 1435 1585"> Date</div></div>
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